(12) **United States Patent**
Nakagawa

(10) **Patent No.: US 6,368,916 B1**
(45) **Date of Patent: Apr. 9, 2002**

(54) **METHOD FOR FABRICATING NONVOLATILE SEMICONDUCTOR MEMORY DEVICE**

(75) Inventor: **Shinichi Nakagawa**, Kawasaki (JP)

(73) Assignee: **Fujitsu Limited**, Kawasaki (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/534,507**

(22) Filed: **Mar. 24, 2000**

(30) **Foreign Application Priority Data**

Oct. 22, 1999 (JP) 11-300401

(51) **Int. Cl.**[7] **H10L 21/336**
(52) **U.S. Cl.** **438/257**; 438/297; 257/316
(58) **Field of Search** 438/257, 258, 438/266, 301–305, 297, 527, 528; 257/316, 324, 314

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,514,889 A * 5/1996 Cho et al. 257/316
5,768,192 A 6/1998 Eitan
5,913,122 A * 6/1999 Lee et al. 438/297

* cited by examiner

Primary Examiner—David Nelms
Assistant Examiner—Dung A Le
(74) *Attorney, Agent, or Firm*—Armstrong, Westerman & Hattori, LLP

(57) **ABSTRACT**

The method for fabricating a nonvolatile semiconductor memory device comprises the step of forming an insulation film **14** on a semiconductor substrate **10**; the step of introducing an impurity into the semiconductor substrate through the insulation film **14** to form a source/drain diffused region **20** and a pocket layer **18**; the step of removing the insulation film **14**; the step of forming a charge storage layer **28** on the semiconductor substrate **10**; and forming gate electrode **40** on the charge storage layer **28** between the source/drain diffused layer **20**. Whereby damage due to the ion implantation is not introduced into the charge storage layer. Thus, deterioration of cycling characteristics and data retention characteristics of the nonvolatile semiconductor memory device can be prevented.

15 Claims, 16 Drawing Sheets